What is claimed is:

1. A test circuit for an integrated circuit comprising a plurality of macro blocks, the test circuit comprising:

a first selector having a first input to which an output signal from a first macro block is input and a second input to which a test input signal for a second macro block is input; and

a second selector having a first input to which an output signal from the first selector is input and a second input to which an output signal from the second macro block is input,

wherein during a first test mode for testing the first macro block, the first selector outputs to the first input of the second selector the output signal that has been input from the first macro block to the first input of the first selector, and the second selector outputs to the first macro block the output signal that has been input from the first selector to the first input of the second selector, and

wherein during a second test mode for testing the second macro block, the first selector outputs to the second macro block the test input signal for the second macro block that has been input to the second input of the first selector, and the second selector outputs the output signal from the second macro block that has been input to the second input of the second selector, as a test output signal for the second macro block.

2. The test circuit as defined in claim 1,

wherein a scan path is set for the test circuit together with the first macro block, and

wherein the first test mode is a scan mode in which testing is performed by a scan method that uses the scan path.

3. The test circuit as defined in claim 2,

wherein, when the number of the output signals from the first macro block to the test circuit is I and the number of input signals from the test circuit to the first macro block is J (where I > J, and I and J are integers greater than or equal to two), the test circuit further comprises (I-J) dummy scan flip-flops to hold (I-J) output signals among the I output signals from the first selector, and

wherein the dummy scan flip-flops output the held output signals through the scan path in the scan mode.

4. The test circuit as defined in claim 1, further comprising:

a test buffer which stores an M-bit test input signal for the second macro block by receiving a K-bit test input signal at a time via K test input terminals (where M > K, and M and K are integers greater than or equal to two), and outputs the stored test input signal to the first selector.

5. The test circuit as defined in claim 1,

wherein the second macro block is a macro block that comprises a physical-layer circuit for data communications,

wherein the test circuit comprises a communications sequencer for performing transmission and reception processing to and from the second macro block by a predetermined communications protocol, and

wherein in the second test mode, the communications sequencer operates to perform processing to transmit a transmission data signal to the second macro block through the first selector, and processing to receive a reception data signal from the second macro block through the second selector.

6. The test circuit as defined in claim 5, further comprising:

a test transmission buffer which stores the transmission data signal to the second macro block; and

a test reception buffer which stores the reception data signal from the second macro block.

7. The test circuit as defined in claim 6,

wherein the test transmission buffer stores a transmission data signal that is input from a test input terminal,

wherein the communications sequencer performs processing to transmit the stored transmission data signal through the first selector to the second macro block, after the storage of the transmission data signal by the test transmission buffer, and also performs processing to receive the reception data signal from the second macro block that has been set to loopback mode, and

wherein the test reception buffer stores the received reception data signal and outputs the stored reception data signal to the test output terminal.

8. The test circuit as defined in claim 6,

wherein the test transmission buffer receives an N-bit transmission data signal for the second macro block by receiving a K-bit transmission data signal at a time via K test input terminals (where N >K, and N and K are integers greater than or equal to two), and

wherein the test reception buffer stores an N-bit reception data signal from the second macro block and outputs the stored reception data signal by outputting a K-bit reception data signal at a time to K test output terminals.

9. An integrated circuit comprising:

the test circuit as define in claim 1;

the first macro block; and

the second macro block.

10. An integrated circuit comprising:

the test circuit as define in claim 2;

the first macro block; and

the second macro block.

11. An integrated circuit comprising:

the test circuit as define in claim 3;

the first macro block; and

the second macro block.

12. An integrated circuit comprising:

the test circuit as define in claim 4;

the first macro block; and

the second macro block.

13. An integrated circuit comprising:

the test circuit as define in claim 5;

the first macro block; and

the second macro block.

14. An integrated circuit comprising:

the test circuit as define in claim 6;

the first macro block; and

the second macro block.

15. An integrated circuit comprising:

the test circuit as define in claim 7;

the first macro block; and

the second macro block.

16. An integrated circuit comprising:

the test circuit as define in claim 8;

the first macro block; and

the second macro block.

17. A test method that uses a test circuit comprising a first selector having a first input to which an output signal from a first macro block is input and a second input to which a test input signal for a second macro block is input, and a second selector having a first input to which an output signal from the first selector is input and a second input to which an output signal from the second macro block is input,

wherein during a first test mode for testing the first macro block, the output signal from the first macro block that has been input to the first input of the first selector is output to the first input of the second selector, and the output signal from the first selector that has been input to the first input of the second selector is output to the first macro block, and

wherein during a second test mode for testing the second macro block, the test input signal for the second macro block that has been input to the second input of the first selector is output to the second macro block, and the output signal from the second macro block that has been input to the second input of the second selector is output as a test output signal for the second macro block.

18. The test method as defined in claim 17,

wherein a scan path is set for the test circuit together with the first macro block, and

wherein testing is performed in scan mode by a scan method that uses the scan path, in the first test mode.

19. The test method as defined in claim 18,

wherein, when the number of the output signals from the first macro block to the test circuit is I and the number of input signals from the test circuit to the first macro block is J (where I > J, I and J are integers greater than or equal to two), (I-J) output signals among the I output signals from the first selector are held, and

wherein the held output signals are output through the scan path in the scan mode.

20. The test method as defined in claim 17,

wherein the test circuit comprises a communications sequencer for performing transmission and reception processing to and from the second macro block by a predetermined communications protocol, and

wherein in the second test mode, the communications sequencer is used to transmit a transmission data signal to the second macro block through the first selector and receive a reception data signal from the second macro block through the second selector.